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MOSCONE WEST CENTER

SAN FRANCISCO, CA, USA

Advanced DFT method using Checker and Indication FFs on Automotive NAND Flash Memory

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Motivation

- The rapid development of automotive electronics
- It is very difficult to achieve with the existing ~98% Test coverage in automotive vehicles

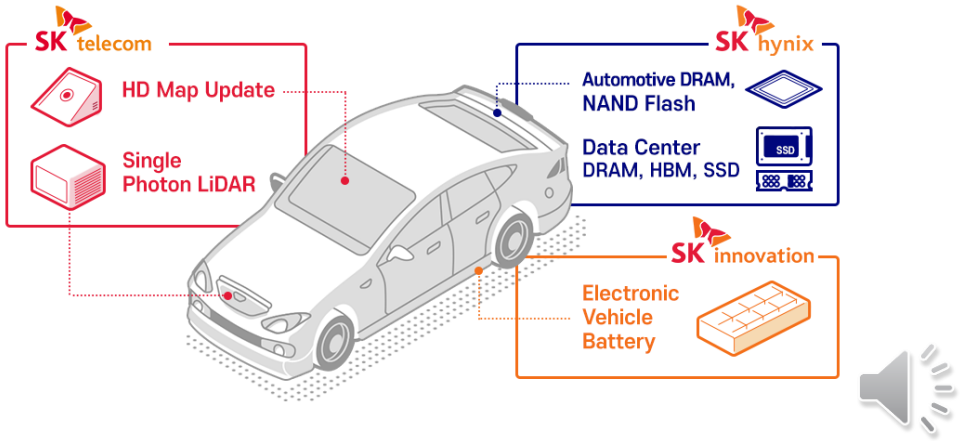
  -> A reliability of <1 DPPM level must be guaranteed

More reliable solution is required !

[Estimated Density and Storage Type]

Application		'20	'23	'25	'30
IVI (In-Vehicle Infotainment)	Density	~64/128GB	~128/256GB	~256/512GB	~512/1TB
	Storage	eMMC	UFS	UFS	UFS
Autonomous (ADAS)	Level	~Lv.2(ADAS)	Lv.3	Lv.4	Lv.5
		Partial	Conditional	High	Full
	Density	8~64GB	~128/256GB	~512GB/1TB	~1TB/2TB↑
	Storage	eMMC	UFS	SSD	

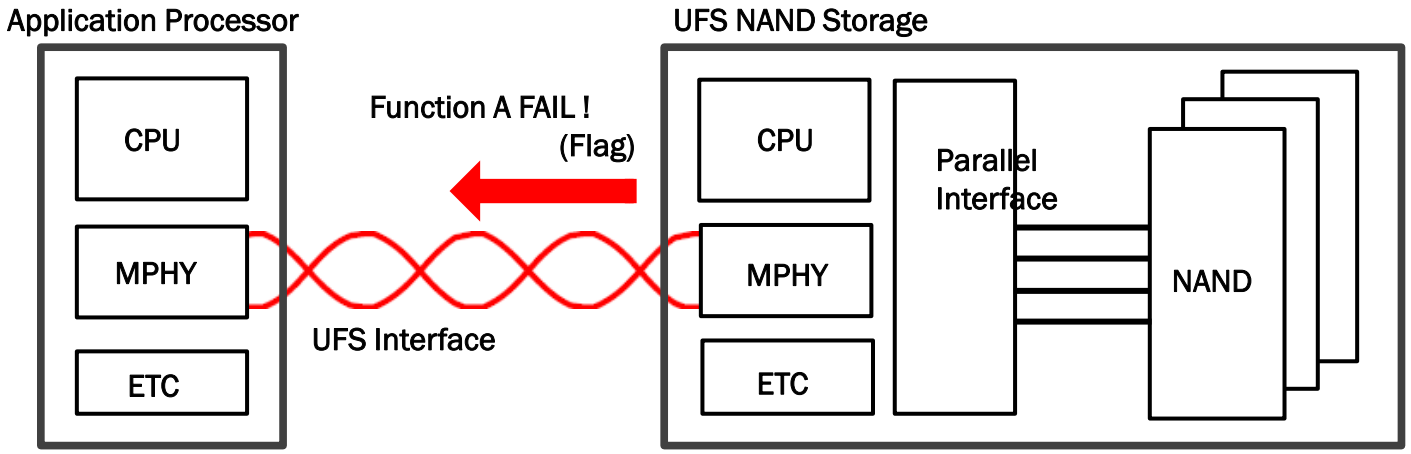
[SK Mobility Technology]



Error Handling on UFS System

- What if failure information for each IP could be reported to the AP in real time ?
- Since the automotive environment is network-based, even in the event of a soft error, if you know the exact cause of the failure, you can temporarily respond with surrounding data.

[Error handling example of Universal Flash Storage (UFS) system]

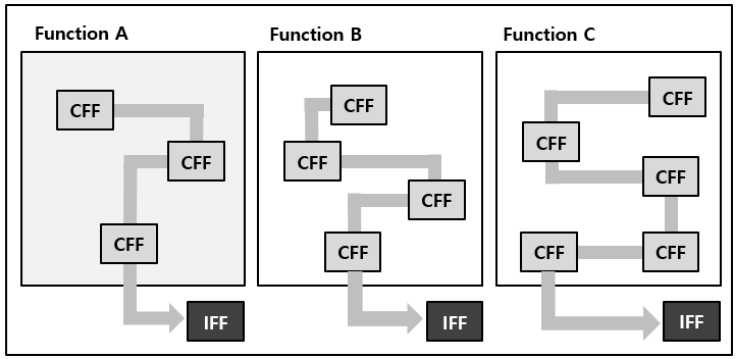


Concept of Checker FF and Indication FF

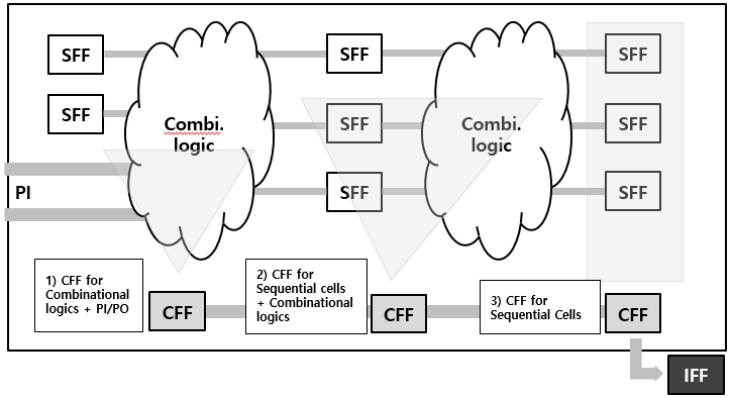
- Automotive SoC design method
  1. Definition of Function
  2. Checker Flip-flop
  3. Indication Flip-flop

- Detail Diagram for Function A
  1. Usage of Checker FF
  2. PI/PO + CFF configuration
  3. Additional observing point in HDL coding level
  4. CFF for sequential cells

(a) Checker flip-flop (CFF) and indication flip-flop (IFF)



(b) Detail block diagram for Function A

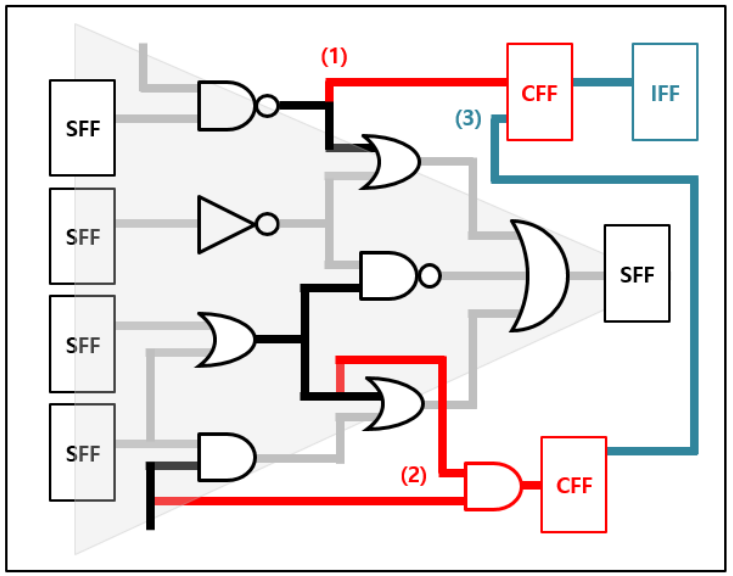


Proposed Method and Usage of CFFs and IFFs

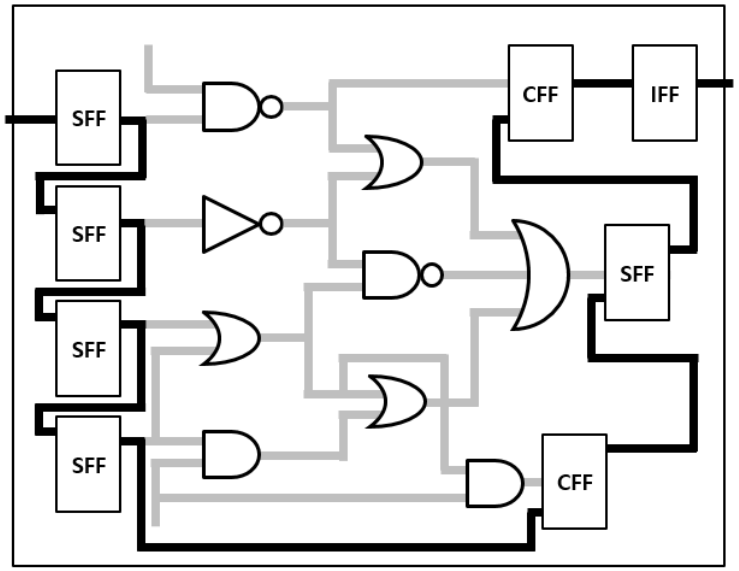
- After checking the CFF set in which all assigned mandatory functions are reviewed, the FF capable of monitoring the corresponding wire is inserted.

  -> It is possible to use the existed scan FF + CFF + IFF

[Functional coverage diagram for CFF/IFF]



[Scan configuration and stitching for CFF/IFF]



Results

- The automotive SoC used in NAND flash memory
- Scan stitching using Synopsys-DC
- Functional coverage : in-house tool
- Test coverage : Synopsys-TMAX

[Experimental device information]

	Device 1	Device 2
Total instances	1,476,890	2,561,335
Scan design	At-speed compressed	At-speed compressed
Scan length	300 / comp. CH	350 / comp. CH
Test pattern	30k w/ power budget	42k w/ power budget
Scan cell area (nm^2)	63,754.72	98,818.79
MBIST cell area (nm^2)	328,693.22	404,371.24
MBIST configuration	18-BIST controller / 67 collars	22-BIST controller / 82 collars

[Comparison of additional hardware overhead and coverage]

	Normal scan insertion Using Synopsys DC		**Test point insertion to enhance observability using Synopsys DC**				**Proposed method to enhance reliability using CFFs and IFFs, and achieved mandatory functional coverage**			
	Scan cell area (nm^2)	Test coverage	Test point area (nm^2)	Test coverage	Hardware overhead (%)	Mandatory functional coverage (%)	CFF and IFF area (nm^2)	Test coverage	Hardware overhead (%)	Mandatory functional coverage(%)
IP1	5,879.64	99.21	347.21	99.67	5.90	62.42	846.29	99.32	14.40	100.00
IP2	8,247.82	97.54	1,541.61	98.92	18.69	66.68	1,324.20	98.72	16.05	99.02
IP3	11,647.32	98.63	2,272.34	99.34	19.50	65.32	3,347.21	98.82	23.73	99.94
IP4	15,279.10	98.59	3,132.28	99.62	20.50	56.96	3,874.65	99.27	25.35	99.84
Device 1	63,754.72	98.02	11,274.22	99.18	17.68	53.72	19,564.32	98.72	30.68	90.71
Device 2	98,818.79	98.06	22,578.69	99.02	22.84	48.22	31,284.74	98.96	31.65	90.32

Summary

- Automotive requires a new SoC design approach
- The proposed method presents a methodology that informs the status quickly and prevents problems from occurring during central processing.(This is also applicable to soft errors)
- Existing test methodologies can be extended and applied to the SoC design stage.
- By using ~30% of additional hardware, very high functional coverage and test coverage were secured.